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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No: 10/637,848

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Filed: August 7, 2003

For: "USE OF SILICON
BLOCK PROCESS STEP TO
CAMOUFLAGE A FALSE
TRANSISTOR"

Croup Art No.: 2814

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Examiner: Cao, Phat X

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Re: RESPONSE TO OFFICE

ACTION

Our Ref: B-4505NP 620843-6/RPB

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Date: May 12, 2005

RESPONSE TO OFFICE ACTION

Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

Dear Sir:

This paper is filed in response to the official action dated March 17, 2005. <u>All</u> amendments and remarks herein are made without prejudice.

<u>Amendments to the claims</u> are reflected in the listing of claims which begins on page 2 of this paper.

Remarks begin on page 3 of this paper.

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